disabling of the cells 100 occurs because each cell 100 reverses the phasing of the data flow. For example, each cell 100 receives the bits of a particular data set on positive clock edges and retransmits the bits of that data set on negative clock edges. The arrangement that is depicted in Fig. 7 is used to disable the flow of bits for the data set that is associated with the DATA2 signal. However, alternatively, to disable the bits for the data set that is associated with the DATA1 signal, the enable input terminals 113 of the cells 200 and 100b are asserted, and the enable input terminals 113 of the cells 100a are de-asserted.

Please replace the paragraph beginning on line 4 of page 9 with the following:

Referring to Fig. 8, as an example, the cell 200 (and/or the cell 100) may be used in a semiconductor circuit, such as a processor 252 (a microprocessor, such as a Pentium® microprocessor, as an example), to communicate bits of data between circuits 254, 256, 260 and 262 of the processor 252. In this manner, the cell 200 may communicate data over a wire 258 for two data sets. More specifically, the cell 200 may communicate data for a first data set between the circuit 254 that is located at one end of the wire 258 and the circuit 260 that is located at another end of the wire 268. The cell 200 may also communicate data for a second data set between the circuit 256 that is located at one end of the wire 258 and the circuit 262 that is located at the other end of the wire 268.

In the Claims:

Rewrite claims 16 and 22 as follows:

16. (Amended) The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

22. (Amended) The method of claim 20, wherein the receiving the second indications comprises:

latching the second indications one bit at a time in response to the first mode.